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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,525	10/29/2003	Chieng-Chung Chen	500-004	6390
24002	7590 01/04/2006	EXAMINER		INER
ANTHONY R. BARKUME			PHAN, TRONG Q	
20 GATEWA MANORVILI	Y LANE LE, NY 11949		ART UNIT	PAPER NUMBER
			2827	
			DATE MAILED: 01/04/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

EX

	Application No.	Applicant(s)				
Office Action Commence	10/696,525	CHEN, CHIENG-CHUNG				
Office Action Summary	Examiner	Art Unit				
	TRONG PHAN	2827				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) Responsive to communication(s) filed on 30 November 2005.						
2a)⊠ This action is FINAL. 2b)□ This	☐ This action is FINAL. 2b)☐ This action is non-final.					
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is						
closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4)⊠ Claim(s) <u>1-13</u> is/are pending in the application.						
4a) Of the above claim(s) <u>3-5 and 11</u> is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1,2,6-10,12 and 13</u> is/are rejected.						
7) Claim(s) is/are objected to.	7) Claim(s) is/are objected to.					
8) Claim(s) are subject to restriction and/or election requirement.						
Application Papers						
9) The specification is objected to by the Examiner.						
10) ☐ The drawing(s) filed on is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) ☒ All b) ☐ Some * c) ☐ None of: 1. ☒ Certified copies of the priority documents have been received. 2. ☐ Certified copies of the priority documents have been received in Application No 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage 						
application from the International Bureau (PCT Rule 17.2(a)).						
* See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s)						
1) X Notice of References Cited (PTO-892)	4) Interview Summary					
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	Paper No(s)/Mail Da					

DETAILED ACTION

Claim Rejections - 35 USC § 103

- 1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 2. Claims 1-2, 6-10 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Fig. 1 Prior Art, in view of Nakano, 6,147,923, and Hiratsuka et al., 5,453,707.

Regarding claims 1-2 and 9-10:

What is not shown in Applicant's Fig. 1 Prior Art is the DRAM cell comprising a MOS transistor (it should be noted that the MOS transistor 211 in Figs. 2(A) and 2(B) of the present invention having drain and source connected together, therefore, it is used as a MOS capacitor as well known in the art) and a storage capacitor as recited in claims 1-2 and 9-10.

Nakano, 6,147,923, discloses in Fig. 1 a voltage boosting circuit for providing the boosted voltage to the word line of a memory device including:

a pumping up circuit comprising an NMOS capacitor 13 and a PMOS capacitor 18

connected in series between to boosted voltage VOUT and the output of inverter 32;

(it should be noted that, in an initial state, only inverter 32 driving both NMOS capacitor 13 and PMOS capacitor 18 to the on-state)(see lines 37-56, column 4).

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the invention was made to utilize the pumping up circuit comprising NMOS capacitor 13 connected in series with PMOS capacitor 18 in Fig. 1 of Nakano, 6,147,923, for the MOS capacitor 12 in Applicant's Fig. 1 PriorArt for the purpose of providing faster boosting (see lines 5-6, column 2 of Nakano, 6,147,923).

Regarding claims 6-8 and 12-13:

What is not shown in Applicant's Fig. 1 Prior Art, which is modified Nakano, 6,147,923, is the driving circuit consists of a PMOS transistor and a NMOS transistor generating a first clock signal according to a second clock signal and a third clock signal as recited in claims 6-8 and 12-13.

Hiratsuka et al., 5,453,707, discloses in Fig. 4 the teaching of using CMOS inverter 18 consists of PMOS transistor Mp1 and NMOS transistor Mn1 to generate first clock signal 01 according to second clock signal at the output of NAND gate 12 and third clock signal at the output of NOR gate 13 having different phases with each other as shown in Fig. 5.

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the invention was made to utilize the CMOS inverter 18 in Figs. 4-5 of Hiratsuka et al., 5,453,707, for the inverter I3 in Applicant's Fig. 1 Prior Art, which is modified by Nakano, 6,147,923, for the purpose of reducing power dissipation and preventing power source noise and ground noise (see lines 43-49, column 3 of Hiratsuka et al., 5,453,707).

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Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Response to Arguments

4. Applicant's arguments filed on 11/30/05, with respect to the rejection(s) of claims 1-13 under 35 USC 112, first paragraph, and 35 USC 103(a) have been fully considered and are persuasive. Therefore, these rejections set forth in the last office action of 9/29/05 have been withdrawn.

However, upon further consideration, a new ground of rejection has been set forth and made FINAL in view of Applicant's amendment and the newly discovered prior art of Nakano, 6,147,923, as above.

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5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRONG PHAN whose telephone number is (571) 272-1794. The examiner can normally be reached on M-F (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AMIR ZARABIAN can be reached on (571)272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PRIMARY EXAMINER